FAIRCHILD SEMICONDUCTOR®

January 2008

74LCX240
Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.5ns t_{PD} max. (V_{CC} = 3.3V), 10µA I_{CC} max.
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal(1)
- ±24mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Note:

1. To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

General Description

The LCX240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

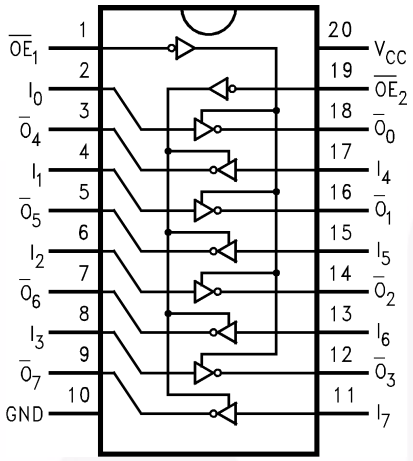
Ordering Information

Order Number	Package Number	Package Description
74LCX240WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX240MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

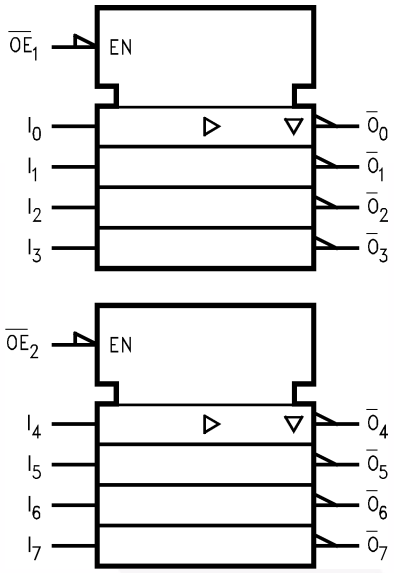
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Diagram



Pin Description

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State(2)	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

2. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions(3)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage			
	Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage			
	3-STATE	0	5.5	V
	HIGH or LOW State	0	V_{CC}	
I_{OH} / I_{OL}	Output Current			
	V_{CC} = 3.0V–3.6V		±24	mA
	V_{CC} = 2.7V–3.0V		±12	
	V_{CC} = 2.3V–2.7V		±8	
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note:

3. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = –40°C to +85°C		Units
				Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V_{IL}	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V_{OH}	HIGH Level Output Voltage	2.3–3.6	I_{OH} = –100µA	V_{CC} – 0.2		V
		2.3	I_{OH} = –8mA	1.8		
		2.7	I_{OH} = –12mA	2.2		
		3.0	I_{OH} = –18mA	2.4		
			I_{OH} = –24mA	2.2		
V_{OL}	LOW Level Output Voltage	2.3–3.6	I_{OL} = 100µA		0.2	V
		2.3	I_{OL} = 8mA		0.6	
		2.7	I_{OL} = 12mA		0.4	
		3.0	I_{OL} = 16mA		0.4	
			I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	2.3–3.6	$0 \le V_I \le 5.5V$		±5.0	µA
I_{OFF}	Power-Off Leakage Current		V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.3–3.6	$V_I = V_{CC}$ or GND		10	µA
			$3.6V \le V_I, V_O \le 5.5V$[4]		±10	
ΔI_{CC}	Increase in I_{CC} per Input	2.3–3.6	$V_{IH} = V_{CC}$ = 0.6V		500	µA

Note:

4. Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T_A = –40°C to +85°C, R_L = 500Ω						Units
		V_{CC} = 3.3V ± 0.3V, C_L = 50pF		V_{CC} = 2.7V, C_L = 50pF		V_{CC} = 2.5V ± 0.2V, C_L = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay	1.5	6.5	1.5	7.5	1.5	7.8	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.5	8.0	1.5	9.0	1.5	10.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew[5]		1.0					ns

Note:

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

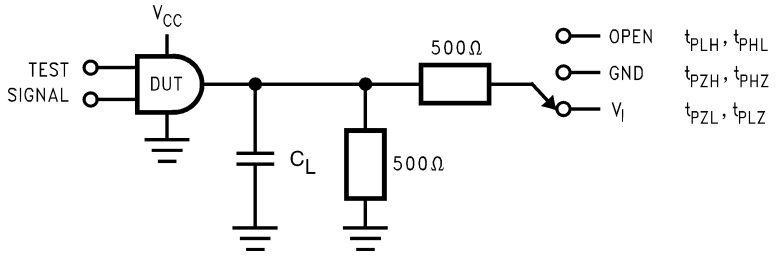
Dynamic Switching Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
		2.5	C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	–0.8	V
		2.5	C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V	–0.6	

Capacitance

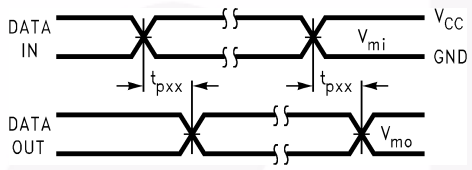
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10MHz	25	pF

AC Loading and Waveforms (Generic for LCX Family)

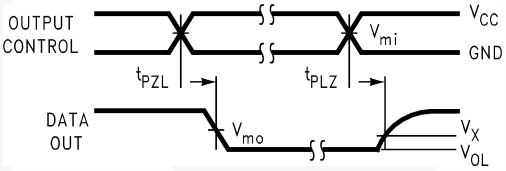


Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND

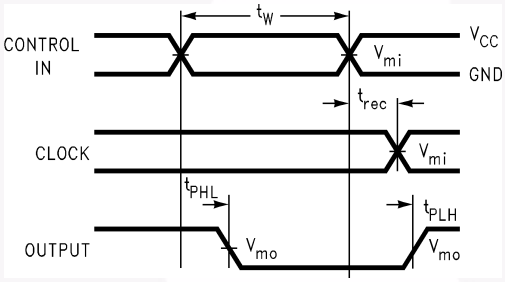
Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)



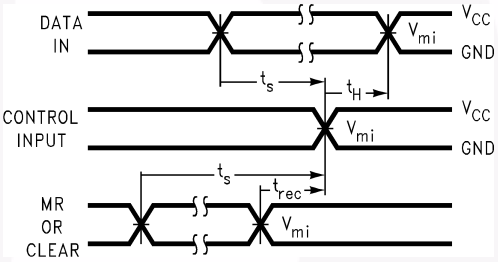
Waveform for Inverting and Non-Inverting Functions



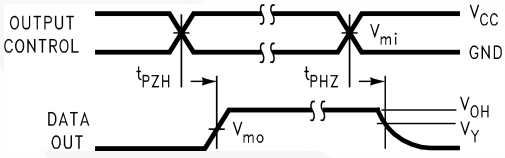
3-STATE Output High Enable and Disable Times for Logic



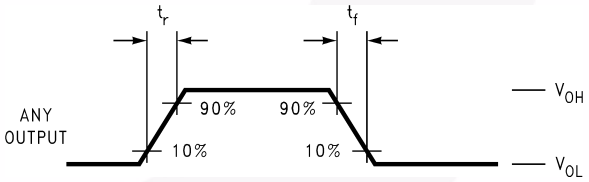
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

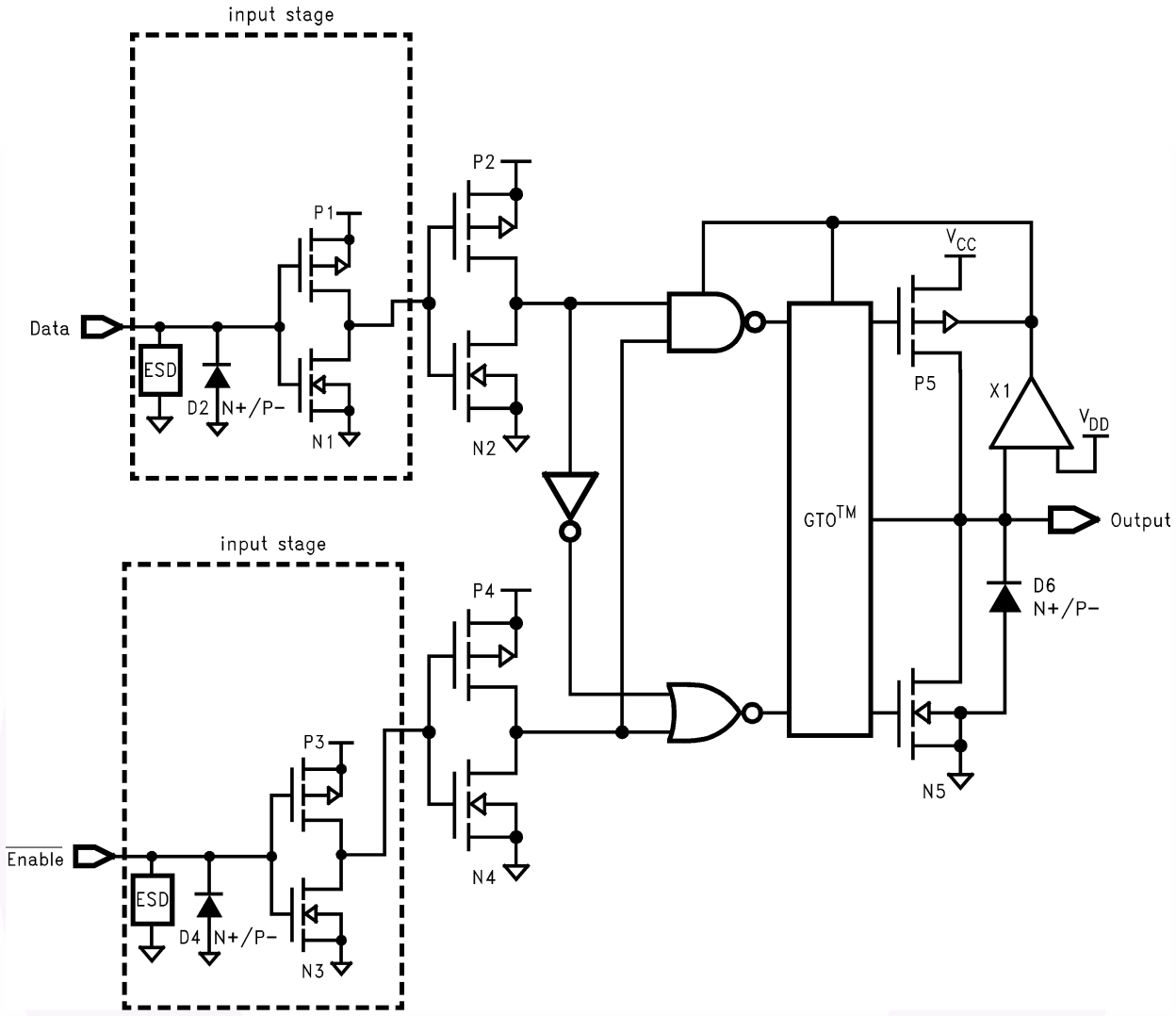


t_{rise} and t_{fall}

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC} / 2
V_{mo}	1.5V	1.5V	V_{CC} / 2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} – 0.3V	V_{OH} – 0.3V	V_{OH} – 0.15V

Figure 2. Waveforms (Input Characteristics; f = 1MHz, t_r = t_f = 3ns)

Schematic Diagram (Generic for LCX Family)



Physical Dimensions

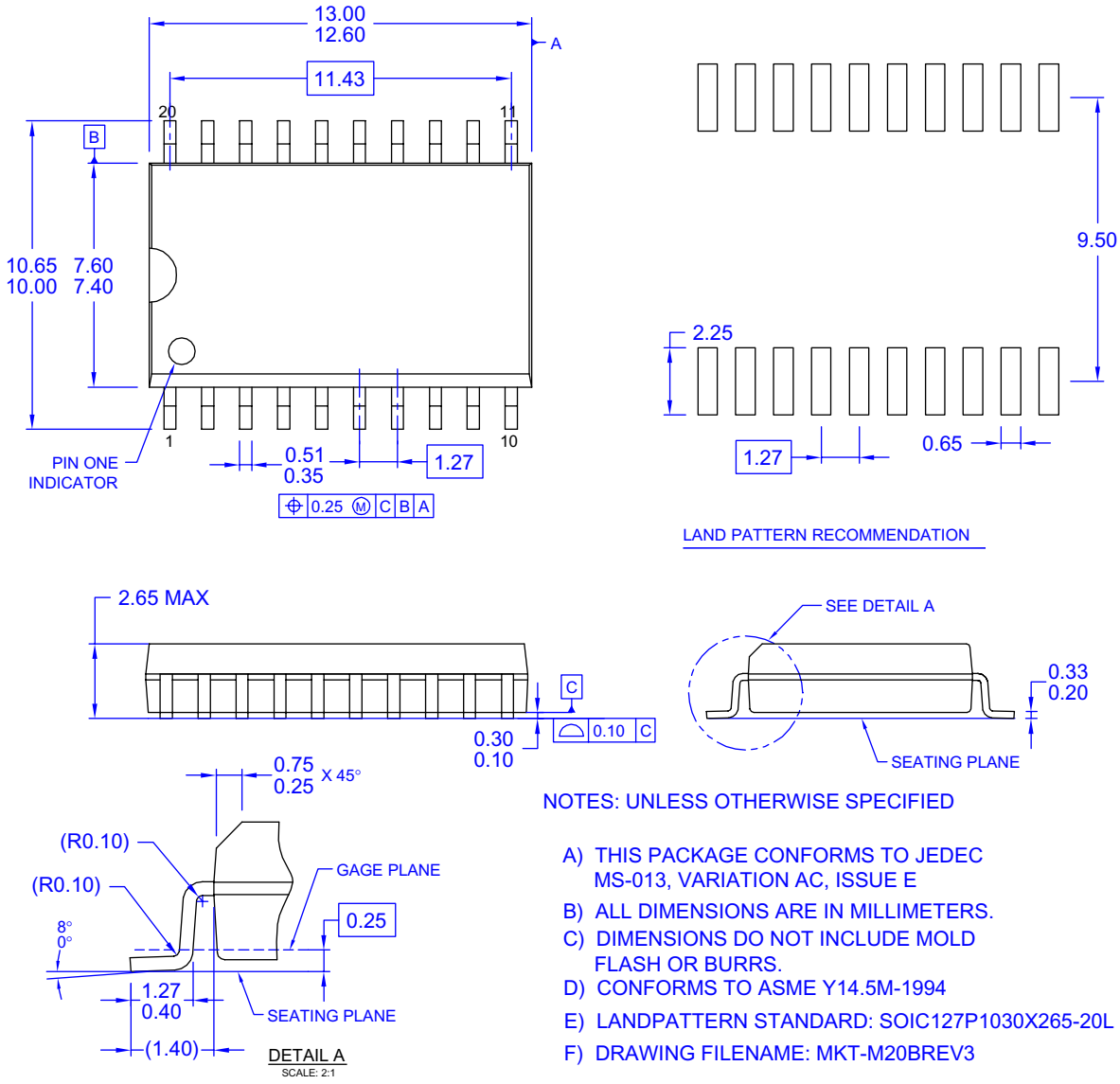


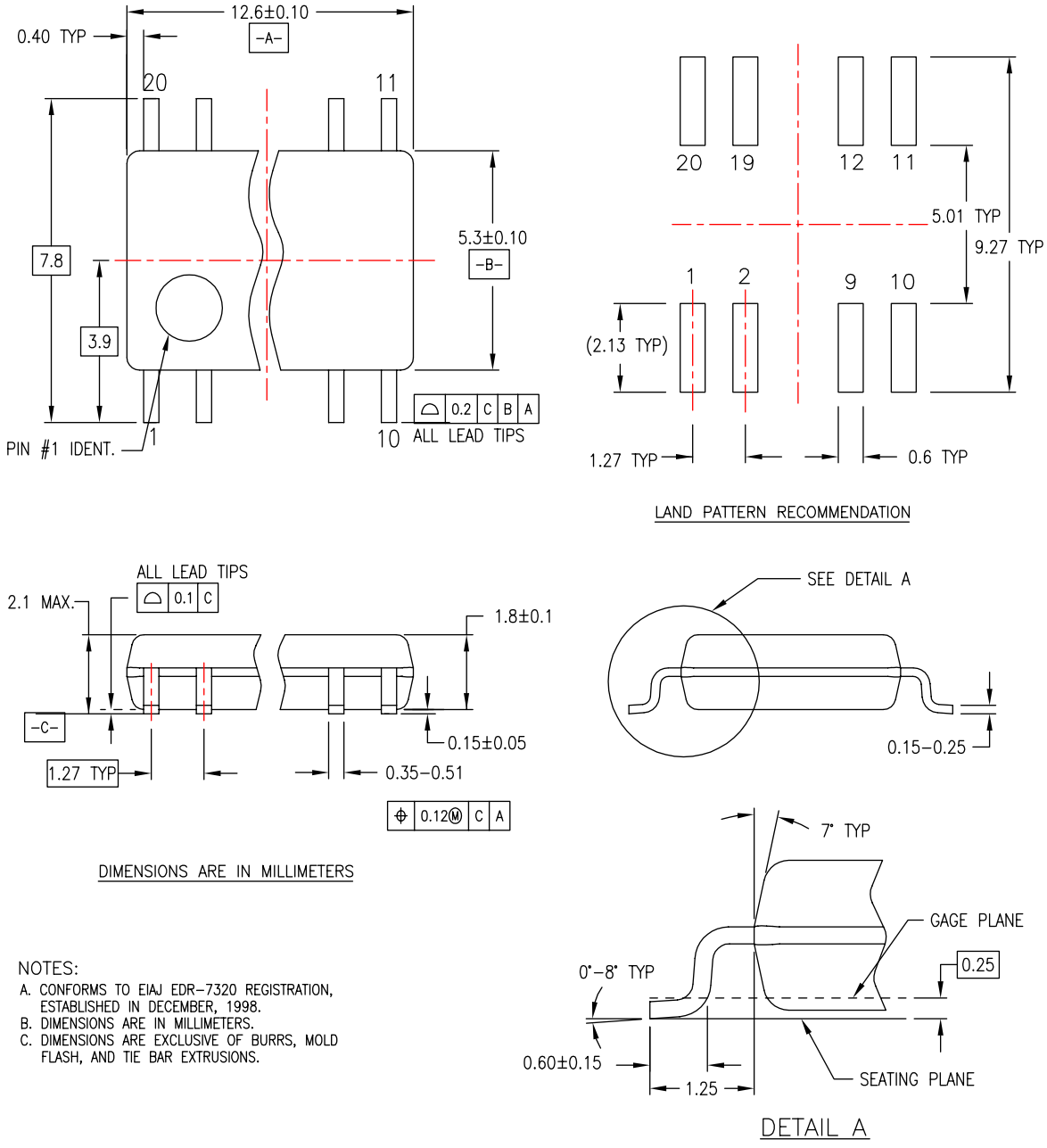
Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

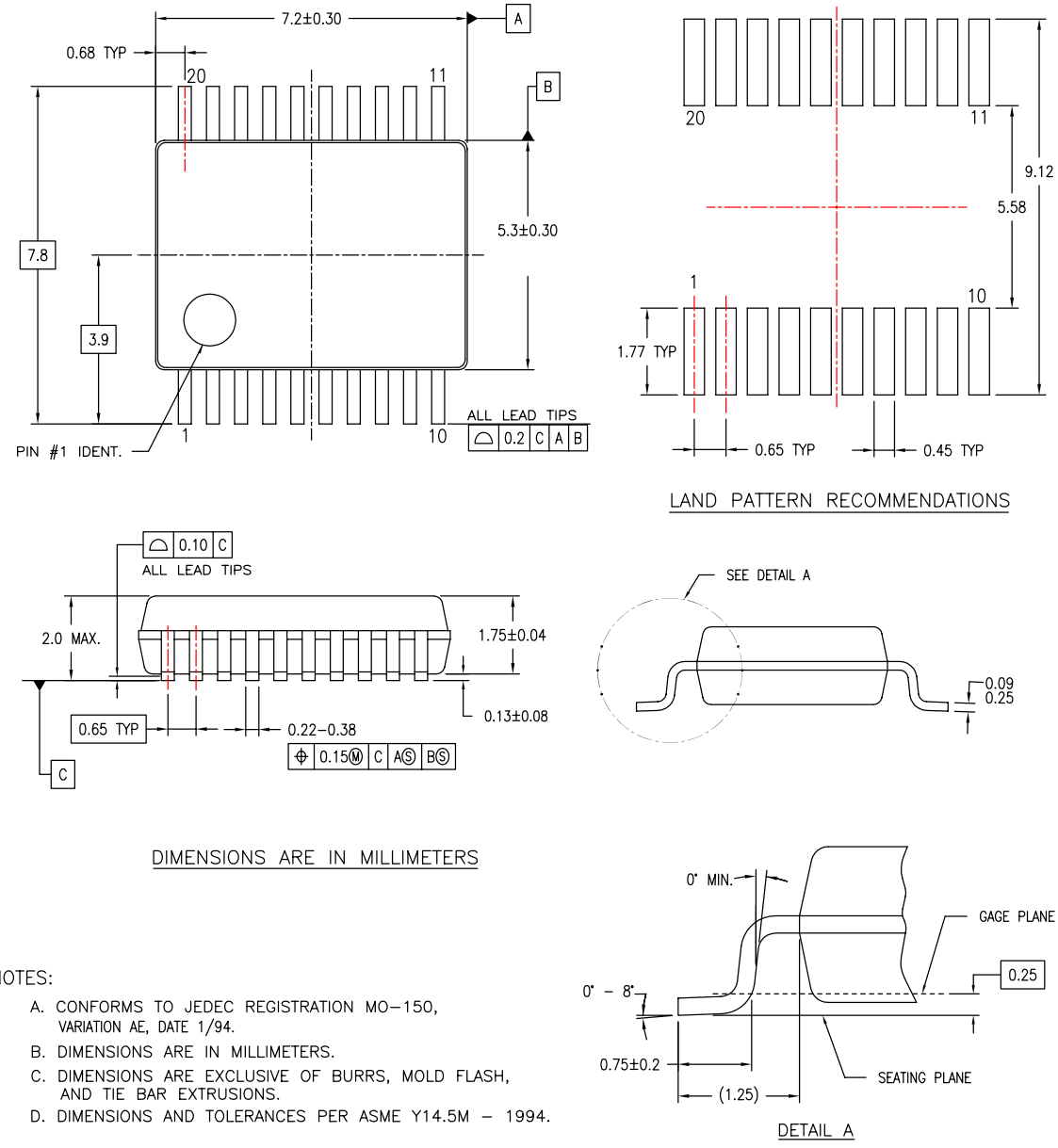
Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

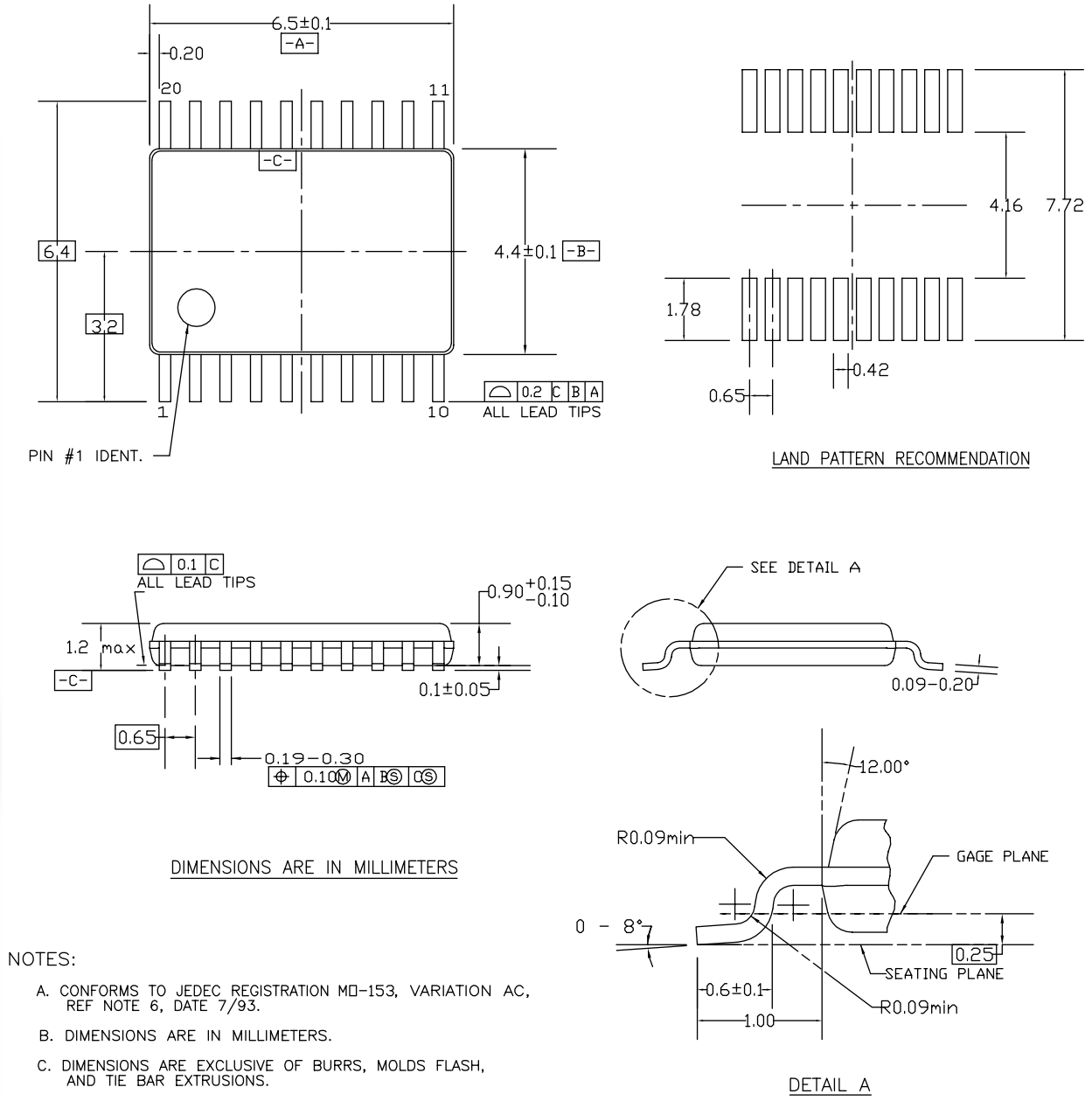
Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 6. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

FAIRCHILD
SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EZSWITCH™ *
™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter® *
FPS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power220®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33